P-Channel JFETs

J174 SST174
J175 SST175
J176 SST176
J177 SST177

Product Summary

Part Number	$V_{GS(off)}$ (V)	$r_{DS(on)}$ Max (Ω)	$I_{D(off)}$ Typ (pA)	t_{ON} Typ (ns)
J/SST174	5 to 10	85	–10	25
J/SST175	3 to 6	125	–10	25
J/SST176	1 to 4	250	–10	25
J/SST177	0.8 to 2.25	300	–10	25

Features

- Low On-Resistance: J174 <85 Ω
- Fast Switching—t_{ON}: 25 ns
- Low Leakage: –10 pA
- Low Capacitance: 5 pF
- Low Insertion Loss

Benefits

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible “Off-Error,” Excellent Accuracy
- Good Frequency Response
- Eliminates Additional Buffering

Applications

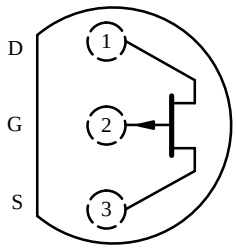
- Analog Switches
- Choppers
- Sample-and-Hold
- Normally “On” Switches
- Current Limiters

Description

The J/SST174 series consists of p-channel analog switches designed to provide low on-resistance and fast switching. This series simplifies series-shunt switching applications when combined with the Siliconix J/SST111 series.

The TO-226AA (TO-92) plastic package provides a low-cost option, while the TO-236 (SOT-23) package provides surface-mount capability. Both the J and SST series are available in tape-and-reel for automated assembly (see Packaging Information).

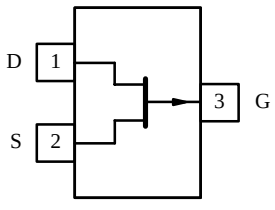
TO-226AA
(TO-92)



Top View

J174
J175
J176
J177

TO-236
(SOT-23)



Top View

SST174 (S4)*
SST175 (S5)*
SST176 (S6)*
SST177 (S7)*

*Marking Code for TO-236

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70257. Applications information may also be obtained via FaxBack, request document #70597.

J/SST174 Series

Absolute Maximum Ratings

Gate-Drain Voltage . . . . . 30 V
Gate-Source Voltage . . . . . 30 V
Gate Current . . . . . –50 mA
Storage Temperature . . . . . –55 to 150°C
Operating Junction Temperature . . . . . –55 to 150°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300°C
Power Dissipation[a] . . . . . 350 mW

Notes
a. Derate 2.8 mW/°C above 25°C

Specifications[a] for J/SST174 and J/SST175

Parameter	Symbol	Test Conditions	Typ[b]	Limits J/SST174 Min	Limits J/SST174 Max	Limits J/SST175 Min	Limits J/SST175 Max	Unit
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA , V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = –15 V, I_D = –10 nA		5	10	3	6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = –15 V, V_{GS} = 0 V		–20	–135	–7	–70	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = –15 V, I_D = –1 mA	0.01					
Drain Cutoff Current	$I_{D(off)}$	V_{DS} = –15 V, V_{GS} = 10 V	–0.01		–1		–1	
		T_A = 125°C	–5					
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS} = 0 V, V_{DS} = –0.1 V			85		125	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = –1 mA , V_{DS} = 0 V	–0.7					V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = –15 V, I_D = –1 mA f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(on)}$	V_{GS} = 0 V, I_D = 0 mA , f = 1 kHz			85		125	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V f = 1 MHz	5					
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = –10 V, I_D = –1 mA f = 1 kHz	20					nV/√Hz
Switching								
Turn-On Time	$t_{d(on)}$	$V_{GS(L)}$ = 0 V, $V_{GS(H)}$ = 10 V See Switching Circuit	10					ns
	t_r		15					
Turn-Off Time	$t_{d(off)}$		10					
	t_f		20					

Notes
a. T_A = 25°C unless otherwise noted. PSCIA
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Pulse test: PW ≤300 µs duty cycle ≤3%.

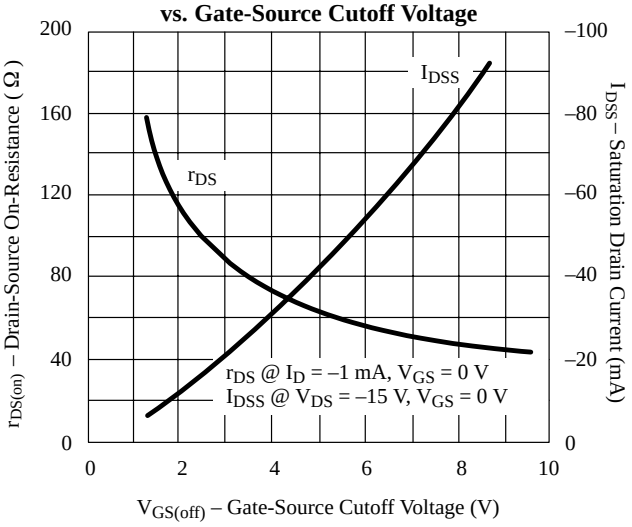
Specifications[a] for J/SST176 and J/SST177

Parameter	Symbol	Test Conditions	Typ[b]	Limits J/SST176 Min	Limits J/SST176 Max	Limits J/SST177 Min	Limits J/SST177 Max	Unit
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA , V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = –15 V, I_D = –10 nA		1	4	0.8	2.25	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = –15 V, V_{GS} = 0 V		–2	–35	–1.5	–20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = –15 V, I_D = –1 mA	0.01					
Drain Cutoff Current	$I_{D(off)}$	V_{DS} = –15 V, V_{GS} = 10 V	–0.01		–1		–1	
		T_A = 125°C	–5					
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS} = 0 V, V_{DS} = –0.1 V			250		300	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = –1 mA , V_{DS} = 0 V	–0.7					V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = –15 V, I_D = –1 mA f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(on)}$	V_{GS} = 0 V, I_D = 0 mA , f = 1 kHz			250		300	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V f = 1 MHz	5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = –10 V, I_D = –1 mA f = 1 kHz	20					nV/√Hz
Switching								
Turn-On Time	$t_{d(on)}$	$V_{GS(L)}$ = 0 V, $V_{GS(H)}$ = 10 V See Switching Circuit	10					ns
	t_r		15					
Turn-Off Time	$t_{d(off)}$		10					
	t_f		20					

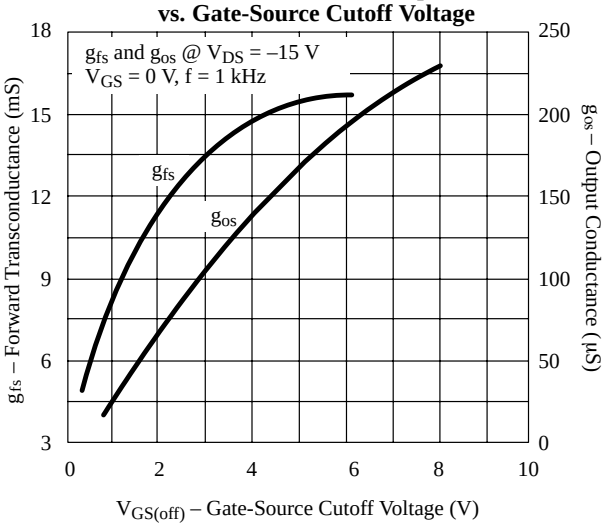
Notes
a. T_A = 25°C unless otherwise noted. PSCIA
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Pulse test: PW ≤ 300 µs duty cycle ≤ 3%.

Typical Characteristics

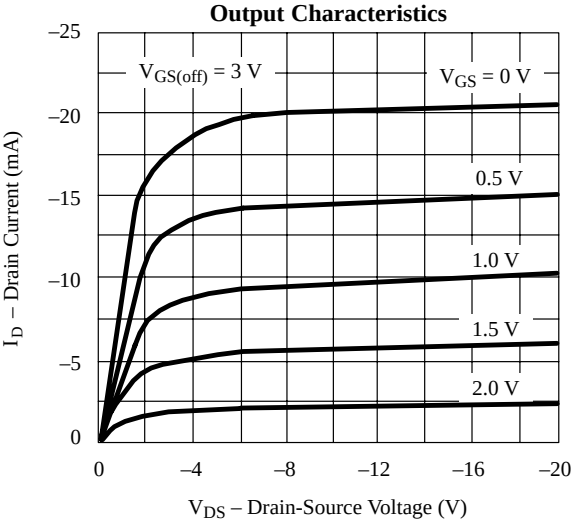
On-Resistance and Drain Current vs. Gate-Source Cutoff Voltage



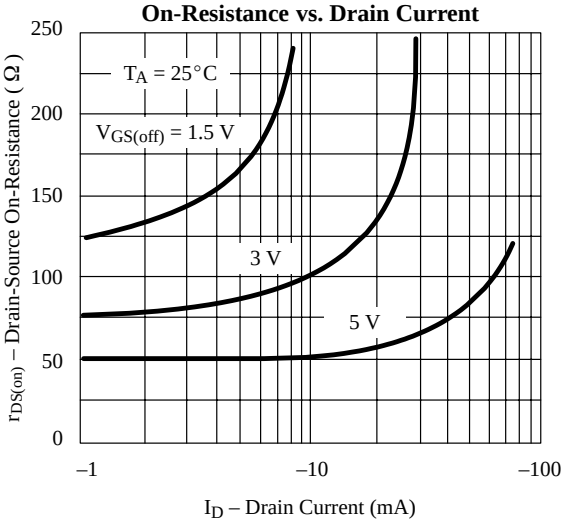
Forward Transconductance and Output Conductance vs. Gate-Source Cutoff Voltage



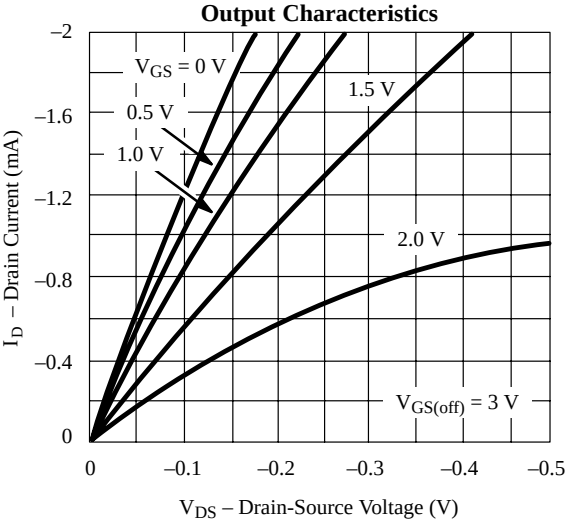
Output Characteristics



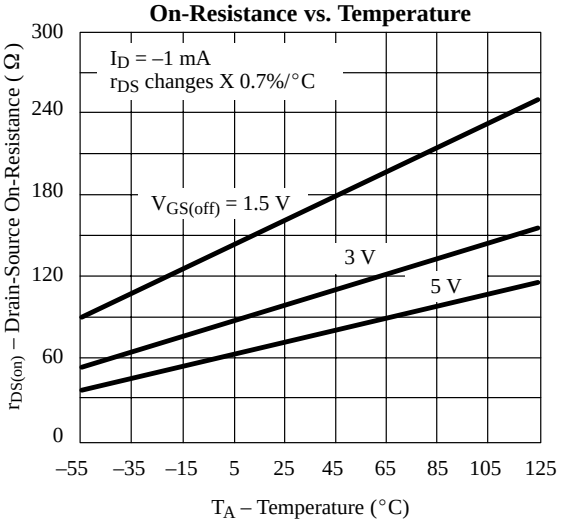
On-Resistance vs. Drain Current



Output Characteristics

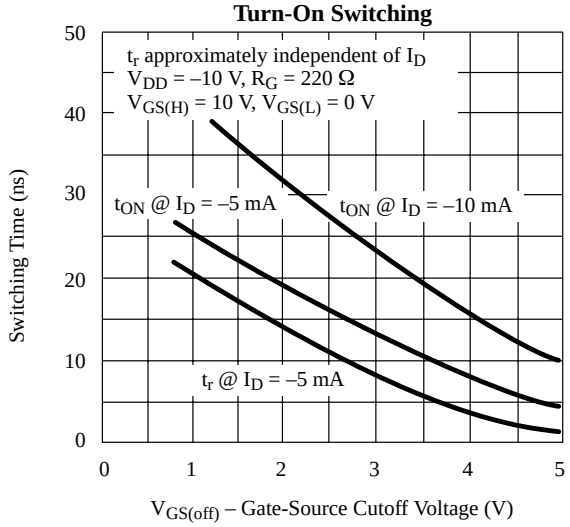


On-Resistance vs. Temperature

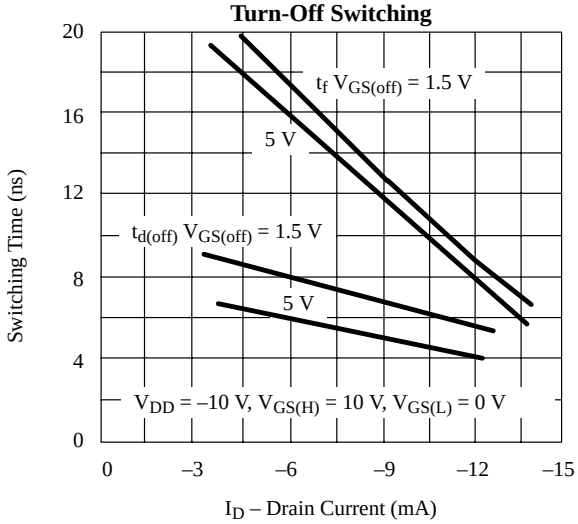


Typical Characteristics (Cont'd)

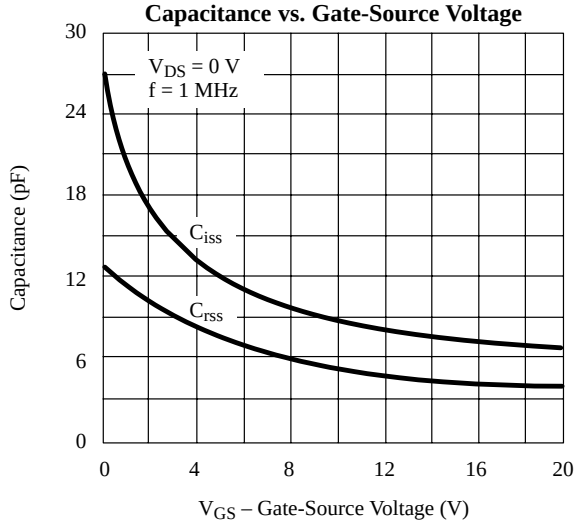
Turn-On Switching



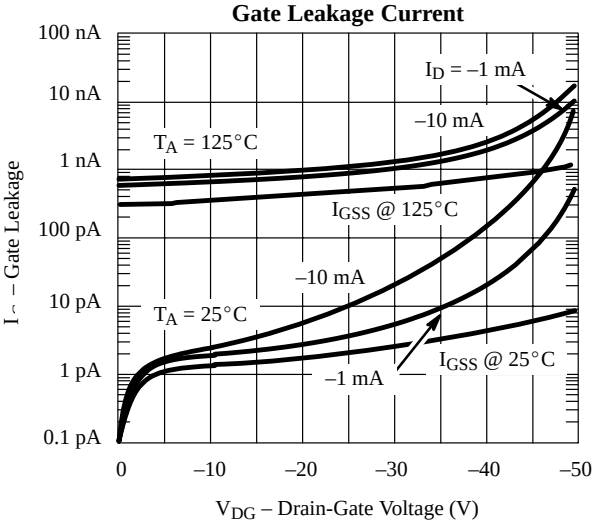
Turn-Off Switching



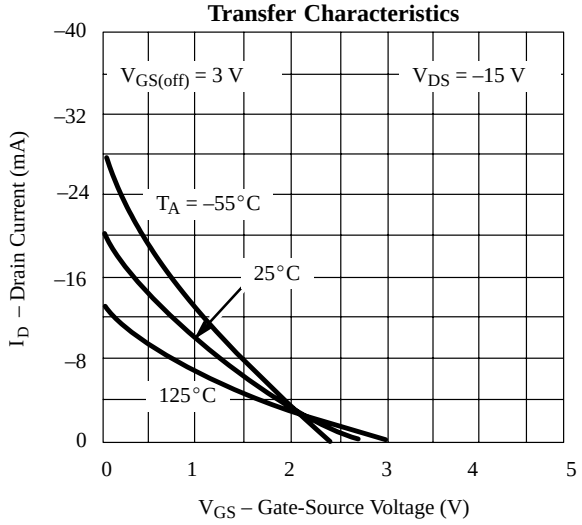
Capacitance vs. Gate-Source Voltage



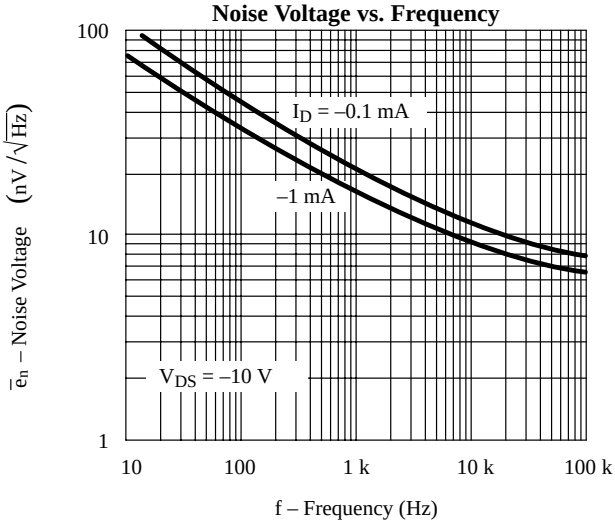
Gate Leakage Current



Transfer Characteristics



Noise Voltage vs. Frequency



Switching Time Test Circuit

	174	175	176	177
V_{DD}	–10 V	–6 V	–6 V	–6 V
V_{GG}	20 V	12 V	8 V	5 V
R_L*	560 Ω	750 Ω	1800 Ω	5600 Ω
R_G*	100 Ω	220 Ω	390 Ω	390 Ω
$I_{D(on)}$	–15 mA	–7 mA	–3 mA	–1 mA

*Non-inductive

Input Pulse

Rise Time < 1 ns
Fall Time < 1 ns
Pulse Width 100 ns
PRF 1 MHz

Sampling Scope

Rise Time 0.4 ns
Input Resistance 10 MΩ
Input Capacitance 1.5 pF

See Typical Characteristics curves for changes.

